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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,945	02/04/2004	Peter J. Fricke	200310842-1	5316
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HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			EXAMINER NADAV, ORI	
			ART UNIT 2811	PAPER NUMBER
			NOTIFICATION DATE 04/10/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/772,945	<b>Applicant(s)</b> FRICKE ET AL.
	<b>Examiner</b> Ori Nadav	<b>Art Unit</b> 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 08 January 2008.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-6,8-33 and 36-59 is/are pending in the application.

4a) Of the above claim(s) 2,12-15,17-25,36,37,42-46 and 50-54 is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1,3-6,8-11,16,26-33,38-41,47-49 and 55-59 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_

5) Notice of Informal Patent Application

6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "a tunnel junction layer", as recited in dependent claim 5, is unclear as to the structural relationship between the tunnel junction layer and the memory array.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka (4,476,547) in view of Udayakumar et al. (2005/0012126).

Miyasaka teaches in figure 5 and related text a memory array comprising:

- a) a multiplicity of row conductors WL and a multiplicity of column conductors BL, the row conductors and column conductors being arranged to cross at cross-points, and
- b) a memory cell C disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor (column 1, lines 63-67).

Miyasaka does not teach that each control element including a tunnel junction and a silicon-rich oxide insulator.

Udayakumar et al. teach in figure 7F and related text a memory cell Cfe having exactly two terminals and having a storage element and a control element wherein the control element including a tunnel junction and a silicon-rich oxide insulator SILOX2.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tunnel junction and a silicon-rich oxide insulator in each control element of Miyasaka's device in order to make an operable device and in order to improve the characteristics of the device, respectively. The combination is motivated by the teachings of Udayakumar et al., who points out the advantages of using a silicon-rich oxide insulator (see e.g. paragraph [0007]).

Regarding the claimed limitations of "each control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon-rich oxide insulator injects current into the tunnel junction when the memory cell is selected", these features are inherent in prior art's device, because prior art's structure is identical to the claimed structure. Note that a recitation of the intended use of the claimed invention must result

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in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the silicon-rich oxide insulator to inject current into the tunnel junction when the memory cell is selected in order to use Miyasaka's device in an application which requires tunneling.

Regarding claim 4, prior art's device includes the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells.

Regarding claims 5-6 and 8-10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises a tunnel junction, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer, a chalcogenide, in prior art's device in order to use known memory control and storage elements, of which official notice is taken.

Regarding claim 5, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tunnel junction layer thickness of about 3-5 nanometers in order to use Miyasaka's device in an application which requires tunneling.

Regarding claim 11, Miyasaka teaches in figure 5 and related text a row conductors are arranged in mutually orthogonal relationship with the column conductors.

Regarding claim 16, prior art's device includes a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

Regarding claim 26, prior art's device includes a tunnel-junction layer SiN over the silicon rich insulator and a second conductive layer 128 over the tunnel-junction layer. Prior art does not state that the memory cell is formed by a method of  
b) depositing and patterning a first conductive layer over the substrate, and  
c) forming and patterning a second conductive layer,

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by

process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 38, prior art's device includes a first interlayer dielectric over the storage layer (122 in Udayakumar et al., figure 7F), and having an opening through the first interlayer dielectric and extending to the storage layer, and having a conductive material therein as a middle electrode 124, this conductive layer is contiguous with the storage layer.

Prior art does not state that the memory cell is formed by a method of

- b) depositing and patterning a first conductive layer over the substrate, and
- c) forming and patterning a second conductive layer,
- d) forming and patterning first and second interlayer dielectrics over the storage layer,
- e) forming an opening through the first interlayer dielectric and extending to the storage layer,
- g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 30, 47 and 55, prior art's device includes a second interlayer dielectric (126 in Udayakumar et al., figure 7F), is formed over the storage layer, forming vias as required through the second interlayer dielectric to selectively interconnect memory cells of the memory arrays.

Prior art does not state that the memory cell is formed by a method of

- b) depositing and patterning a first conductive layer over the substrate, and
- c) forming and patterning a second conductive layer,
- d) forming and patterning first and second interlayer dielectrics over the storage layer,
- e) forming an opening through the first interlayer dielectric and extending to the storage layer,
- g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.
- k) forming vias as required through the second interlayer dielectric, and repeating steps b) through k) until a desired number of memory array layers have been formed.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 27-29, 31-33, 39-41, 48-49 and 56-57, Miyasaka teaches a memory array comprising a multiplicity of the memory cells, a substrate carrying electronics and an IC comprising a multilayer memory, wherein a multiplicity of the memory arrays are arranged in memory layers.

Regarding claims 58-59, Miyasaka teaches in figure 5 and related text the two terminals of the two terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

***Response to Arguments***

Applicant argues that the motivation to combine is "overly conclusory and general".

The examiner stated that "It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tunnel junction and a silicon-rich oxide insulator in each control element of Miyasaka's device in order to make an operable device and in order to improve the characteristics of the device, respectively. The combination is motivated by the teachings of Udayakumar et al., who points out the advantages of using a silicon-rich oxide insulator". That is Udayakumar et al. teach that a silicon-rich oxide insulator is an "effective barrier to the diffusion of hydrogen" (see e.g. paragraph [0007]). Clearly, using an effective barrier in Miyasaka's device would improve the device characteristics. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tunnel junction and a silicon-rich oxide insulator in each control element of Miyasaka's device, as claimed.

Applicant argues that "the capacitor portion of the Miyasaka device is the storage element of the dynamic RAM device described in the Miyasaka reference and, thus, even if the Udayakumar reference teaches a tunnel junction and a silicon-rich oxide insulator associated with a capacitor, these features are directed at the storage portion of the Miyasaka device, not the control element, as recited in independent claim 1 of the present disclosure".

The combined structure of Miyasaka and Udayakumar is identical to the claimed structure. Therefore, it is unclear to the examiner why the elements in Miyasaka and Udayakumar's structure (e.g. "control element") cannot be called the same names as in the claimed structure.

Applicant argues that prior art does not teach a silicon-rich oxide insulator injects current into the tunnel junction and such limitation is not an intended use of the claimed invention, because of the particular configuration required (thin Alox).

The recitation of the silicon-rich oxide insulator injects current into the tunnel junction is an intended use of the claimed invention, because an artisan would understand that using the silicon-rich oxide insulator to inject current into the tunnel will require specific Alox thickness. This recitation must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Applicant argues that the storage element and the control element of the present disclosure are distinct elements serving different functions, because "Figure 2 of the present application shows the storage element 50 to be separate and distinct from the silicon-rich insulator 60 that, in combination with the distinct tunnel junction 70, contributes to formation of the control element 45". Applicant further argues that the specification of the present disclosure recites, "Silicon-rich insulator 60 may be considered an electronic switch that allows selection of the memory cell for programming and sensing the storage state, as well as isolation of the memory cell when the memory cell is unselected." Hence, Applicant respectfully submits that the silicon-rich insulator is not equivalent to a storage element (e.g., a capacitor) because the storage element is separate and distinct (e.g., see independent claim 1 and Figure 2).

Applicant elected the embodiment of figure 3 for examination. The structure of figure 3 comprises a silicon oxide (junction tunnel) formed over an SRO (control element) over ILD and over Chalcogenide material (storage element). The structure of Miyasaka and Udayakumar et al. **comprises** identical elements. Therefore, the structure of Miyasaka and Udayakumar et al. teaches the claimed limitations.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.  
4/8/2008

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